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REMARKS

Prior to the present response, claims 21-34 were pending in the present application, and remain in the present application after the present response. Reconsideration and allowance of pending claims 21-34 in view of the following remarks are requested.

A. Rejection of Claims 21-34 under 35 USC §103(a)

The Examiner has rejected claims 21-34 under 35 USC §103(a) as being unpatentable over U.S. patent application publication number 2005/0079696 to Luigi Colombo (hereinafter "Colombo") in view of U.S. patent number 6,265,260 to Alers et al. (hereinafter "Alers"), or U.S. patent no. 6,566, 250 to Tu et al. (hereinafter "Tu") as evidenced by U.S. patent application publication number 2004/0188240 to Chang et al. (hereinafter "Chang '240"), or U.S. patent number 6,090,210 to Ballance et al. (hereinafter "Ballance"), or U.S. patent number 6,759,337 to Aronowitz et al. (hereinafter "Aronowitz"), or U.S. patent application publication number 2005/0019964 to Chang et al. (hereinafter "Chang '964"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claims 21 and 28, is patentably distinguishable over the cited references, either singly or in any combination.

As disclosed in the present application, in an embodiment of the present invention, gate stack 102 can be formed in a process chamber by utilizing a plasma etch. As disclosed in the present application, a nitridation process can be performed by utilizing a nitrogen plasma to nitridate exposed surfaces of gate stack 102 immediately after the

PAGE 7/13 * RCVD AT 1/21/2008 7:11:02 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-5/10 * DNIS:2738300 * CSID:949 282 1002 * DURATION (mm-ss):02-46

gate etch process has been performed in the same process chamber. The nitridation process can be utilized to repair damage the may occur to gate stack 102 during the etch process and to form a barrier in high-k dielectric segment 106 to prevent oxygen from laterally diffusing into the high-k dielectric segment during subsequent processing steps.

Thus, by performing a nitridation process immediately after the gate etch process, the present invention forms a barrier in high-k dielectric segment 106 immediately after the gate etch process to prevent oxygen form laterally diffusing into the high-k dielectric segment during subsequent processing steps while repairing any damage to the gate stack as a result of the gate etch process. Also, by utilizing a single process chamber to perform the gate stack etch and nitridation processes, as specified in independent claims 21 and 28, the need to break vacuum is avoided, thereby advantageously increasing throughput and reducing manufacturing costs.

In contrast, Colombo specifically discloses performing etch process 330 to form a patterned gate structure with top and sidewall surfaces exposed, removing gate mask 328, forming implant mask 333, performing shallow drain extension dopant implant 334, optionally employing a cleaning operation to expose a sidewall portion of gate dielectric 316, and performing nitridation process 335 to nitride the sidewalls and top of the gate structure. See, e.g., page 4, paragraphs [0028] and [0029] and Figures 5D through 5F of Colombo. However, Colombo fails to disclose performing a nitridation process immediately after etching a gate electrode layer and a high-k dielectric layer, as specified in independent claims 21 and 28. Also, Colombo fails to disclose using a nitrogen

containing plasma to nitridate sidewalls of the high-k dielectric segment, as specified in independent claims 21 and 28. Furthermore, Colombo fails to disclose etching the gate electrode and the high-k dielectric layer and performing the nitridation process in the same plasma process chamber.

On pages 3 and 4 of the Final Rejection of November 19, 2007, the Examiner states that "Colombo [0026] discloses that the process steps in exemplary method in Fig. 4 may occur in different orders" ... therefore, "it would have been obvious to one with ordinary skill in the art that the nitridation process may be performed immediately after the step of etching the gate electrode layer and the high-k dielectric layer as claimed in absence of unexpected result or criticality." However, as disclosed in the present application, after the gate etch, oxygen can laterally diffuse into the high-k gate dielectric during subsequent process steps and alter the properties of the high-k dielectric material and the transistor gate. *See*, e.g., page 2, lines 3-8 of the present application.

Thus, by performing the nitridation process immediately after the step of etching the gate electrode layer and the high-k dielectric layer, the invention as specified by independent claims 21 and 28 advantageously limits the opportunity for oxygen to laterally diffuse into the high-k gate dielectric from subsequent process steps. In contrast, by disclosing that the process steps in the method in Figure 4 may occur in different orders, Colombo teaches away from any specific advantage that may be achieved by performing the nitridation process immediately after the step of etching the gate electrode layer and the high-k dielectric layer, as specified by independent claims 21 and 28.

The Examiner relies on Alers and Tu to show a conventional nitridation method of applying plasma comprising nitrogen. On page 3 of the Final Rejection of November 19, 2007, the Examiner states the "[b]ecause it is a conventional method in the art of semiconductor device fabrication and because it is disclosed by Alers, Tu, hence, it would have been obvious to one of ordinary skill in the art to apply said nitridation method in the process of Colombo in order to efficiently carry out the nitridation process." However, the subject matter of Alers and Tu is significantly different than Colombo. For example, Alers discloses a method for making an integrated circuit capacitor having a relatively high capacitance. *See*, e.g., column 1, line 62-65 of Alers. For example, Tu is directed to a method for forming a self-aligned capping layer over a metal filled feature in a multi-layer semiconductor device. *See*, e.g., the Abstract of Tu. In contrast, Colombo is directed to encapsulation and conditioning structures and techniques for MOS transistor gates. *See*, e.g., page 1, paragraph [0001] of Colombo. Thus, Applicants respectfully submit that a person of ordinary skill in the art would not have a sufficient reason to combine Alers and/or Tu with Colombo, as suggested by the Examiner.

Since Colombo does not specify performing nitridation and etching in the same process chamber, as acknowledged by the Examiner on page 4 of the Final Rejected of November 19, 2007, the Examiner cites Chang '240, Ballanace, Aronowitz, and Chang '964 as evidence that "[i]t is common in the art that the plasma process chamber may be used for performing both etching and nitridation because it is efficient and more cost

effective." However, the structures disclosed in Chang '240, Ballance, Aronowitz, and Chang '964 are significantly different than the transistor gate disclosed in Colombo.

In particular, Chang '240 discloses a process for in-situ nitridation and formation of metal salicides, which are formed by utilizing a plasma generator. *See*, e.g., the Abstract of Chang '240. However, Chang '240 fails to disclose or suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch. Ballance discloses a showerhead for introducing gas from one or more external supplies into a substrate processing chamber. *See*, e.g., the Abstract of Ballance. However, Ballance fails to disclose or suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch.

Aronowitz discloses a process for etching a controllable thickness of oxide formed over a semiconductor substrate by exposing the oxide to a nitrogen plasma in an etch chamber while applying an RF bias to a substrate support on which the substrate is supported in the etch chamber. *See*, e.g., the Abstract of Aronowitz. However, Aronowitz fails to disclose or suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch. Chang '964 discloses a method for determining a composition of an integrated circuit feature on a substrate, including collecting intensity data representative of spectral wavelengths of radiant energy generated by a plasma during plasma nitridation of the integrated circuit feature on the substrate. *See*, e.g., the Abstract of Chang '964. However, Chang '964 fails to disclose or suggest application of its disclosure to plasma nitridation of gate stacks in transistors after a gate etch.

Thus, since the structures disclosed in Chang '240, Ballanace, Aronowitz, and Chang '968 are significantly different than the transistor gate disclosed in Colombo, Applicants respectfully submit that, at the time the invention, as defined by independent claims 21 and 28 was made, a person of ordinary skill in the art would not have a sufficient reason or be sufficiently motivated to combine Chang '240, Ballanace, Aronowitz, and/or Chang '968 with Colombo as suggested by the Examiner.

For the foregoing reasons, Applicants respectfully submit that the present invention, as defined by independent claims 21 and 28 are patentably distinguishable over the cited references, either singly or in any combination thereof. Thus, claims 22-27 depending from independent claim 21 and claims 29-34 depending from independent claim 28 are, *a fortiori*, also patentably distinguishable over the cited references for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. <u>Conclusion</u>

For all the foregoing reasons pending claims 21-34 are patentably distinguishable over the cited art, and an early allowance of pending claims 21-34 is respectfully requested.

Attorney Docket No.: 0180151

Respectfully Submitted,
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Date: 1/21/08

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